Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application :

Listing of Claims:

Claim 1 (Currently amended) : A method for fabricating a mask read-only-memory with diode cells, comprising:

providing a semiconductor substrate;

forming a buried diffusion layer with a first conductivity in [[the]] a top portion of said semiconductor substrate;

forming a plurality of shallow trench isolation regions in said semiconductor substrate and then making said buried diffusion layer to a plurality of bit lines;

forming an interlayer dielectric layer over said buried diffusion layer and said shallow trench isolation regions;

forming a photoresist layer with a mask read-only-memory code pattern on said interlayer dielectric layer;

performing an anisotropic etching process to form openings in said interlayer dielectric layer unto the exposed regions of said buried diffusion layer using said photoresist layer as an etching mask;

removing said photoresist layer;

performing ion implantation to form a diffusion region with a second conductivity opposite to said first conductivity in each of said exposed regions of said buried diffusion layer;

forming a contact plug in each said opening unto said diffusion region; and

forming a conductive layer on said interlayer dielectric layer for serving as word lines.

Claim 2 (Original) : The method of claim 1, wherein said semiconductor substrate is selected from a group consisting of silicon substrate, germanium substrate and germanium arsenic substrate.

Claim 3 (Original): The method of claim 1, wherein said first conductivity is either of N type conductivity and P type conductivity.

Claim 4 (Original) : The method of claim 1, wherein said interlayer dielectric layer comprises silicon dioxide formed by a chemical vapor deposition method.

Claim 5 (Original) : The method of claim 1, wherein said interlayer dielectric layer comprises PSG (phosphosilicate glass) formed by a plasma enhanced chemical vapor deposition method with reaction gases of SiH_4, N_2O and PH_3.

Claim 6 (Original) : The method of claim 1, wherein said interlayer dielectric layer comprises BPSG (borophosphosilicate glass) formed by a plasma enhanced chemical vapor deposition method with reaction gases of TEOS (tetra-ethyl-ortho-silicate), O_3, TEB (tri-ethyl-borate) and TMPO (tri-methyl-phosphate) at a temperature of about 400~500℃ and under a pressure of about 10 torr.

Claim 7 (Original) : The method of claim 1, wherein said interlayer dielectric layer comprises silicon nitride formed by a low pressure chemical vapor deposition method with reaction gases of SiH_2Cl_2 and NH_3 at a temperature of about 700~800℃.

Claim 8 (Original) : The method of claim 1, wherein said interlayer dielectric layer comprises silicon oxynitride formed by a plasma enhanced chemical vapor deposition method with reaction gases of SiH_4, N_2O and N_2.

Claim 9 (Original) : The method of claim 1, wherein said contact plug comprises tungsten formed by a low pressure chemical vapor deposition method with reaction gases of WF_6 and SiH_4 at a temperature of about 300~550℃ and under a pressure of about 1~100 torr.

Claim 10 (Original) : The method of claim 1, wherein said conductive layer comprises polysilicon formed by a low pressure chemical vapor deposition method with a reaction gas of SiH_4 at a temperature of about 600~650℃ and under a pressure of about 0.3~0.6 torr.

Claim 11 (Currently amended) : A method for fabricating a mask read-only-memory with diode cells, comprising:

providing a semiconductor substrate;

forming a buried diffusion layer with a first conductivity in [[the]] a top portion of said semiconductor substrate for serving as bit lines;

forming a doped conductive layer with said first conductivity on said buried diffusion layer, wherein the dopant concentration of said doped conductive layer is lighter than that of said buried diffusion region;

forming a plurality of shallow trench isolation regions in said semiconductor substrate;

forming an interlayer dielectric layer over said doped conductive layer and said shallow trench isolation regions;

forming a photoresist layer with a mask read-only-memory code pattern on said interlayer dielectric layer;

performing an anisotropic etching process to form openings in said interlayer dielectric layer unto the exposed regions of said doped conductive layer using said photoresist layer as an etching mask;

removing said photoresist layer;

performing ion implantation to form a diffusion region with a second conductivity opposite to said first conductivity in each of said exposed regions of said doped conductive layer;

forming a contact plug in each of said openings unto said diffusion region; and

forming a conductive layer on said interlayer dielectric layer for serving as word lines.

Claim 12 (Original) : The method of claim 11, wherein said first conductivity is either of N type conductivity and P type conductivity.

Claim 13 (Original) : The method of claim 11, wherein said doped conductive layer comprises doped polysilicon formed by an in-situ doped low pressure chemical vapor deposition method with a reaction gas of

SiH_4 and a dopant source of PH_3 at a temperature of about 600~650℃ and under a pressure of about 0.3~0.6 torr.

Claim 14 (Original) : The method of claim 11, wherein said interlayer dielectric layer comprises silicon dioxide formed by a chemical vapor deposition method.

Claim 15 (Original) : The method of claim 11, wherein said interlayer dielectric layer comprises PSG (phosphosilicate glass) formed by a plasma enhanced chemical vapor deposition method with reaction gases of SiH_4, N_2O and PH_3.

Claim 16 (Original) : The method of claim 11, wherein said interlayer dielectric layer comprises BPSG (borophosphosilicate glass) formed by a plasma enhanced chemical vapor deposition method with reaction gases of TEOS (tetra-ethyl-ortho-silicate), O_3, TEB (tri-ethyl-borate) and TMPO (tri-methyl-phosphate) at a temperature of about 400~500℃ and under a pressure of about 10 torr.

Claim 17 (Original) : The method of claim 11, wherein said interlayer dielectric layer comprises silicon nitride formed by a low pressure chemical vapor deposition method with reaction gases of SiH_2Cl_2 and NH_3 at a temperature of about 700~800℃.

Claim 18 (Original) : The method of claim 11, wherein said interlayer dielectric layer comprises silicon oxynitride formed by a plasma

enhanced chemical vapor deposition method with reaction gases of SiH_4, N_2O and N_2.

Claim 19 (Original) : The method of claim 11, wherein said contact plug comprises tungsten formed by a low pressure chemical vapor deposition method with reaction gases of WF_6 and SiH_4 at a temperature of about 300~550℃ and under a pressure of about 1~100 torr.

Claim 20 (Original) : The method of claim 11, wherein said conductive layer comprises polysilicon formed by a low pressure chemical vapor deposition method with a reaction gas of SiH4 at a temperature of about 600-650℃ and under a pressure of about 0.3-0.6 torr.